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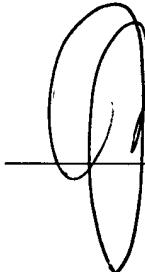
PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional)	
		JAR-829-618	
	Application Number		Filed
	10/720,764		November 25, 2003
	First Named Inventor		YONEMARU
	Art Unit	Examiner	
	2826	DICKEY, T.	

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.



Signature
Joseph A. Rhoa

I am the

Applicant/Inventor

Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

Attorney or agent of record 37,515
(Reg. No.)

Attorney or agent acting under 37CFR 1.34.
Registration number if acting under 37 C.F.R. § 1,34 _____

Typed or printed name

703-816-4043

Requester's telephone number

March 8, 2007

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

*Total of 1 form/s are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

YONEMARU Atty. Ref.: 829-618; Confirmation No. 3114

Appl. No. 10/720,764 TC/A.U. 2826

Filed: November 25, 2003 Examiner: DICKEY, T.

For: SEMICONDUCTOR INTEGRATED LOGIC CIRCUIT INCLUDING TWO PMOS TRANSISTORS CONNECTED IN SERIES AND TWO NMOS TRANSISTORS CONNECTED IN SERIES

* * * * *

March 8, 2007

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Pursuant to the OG Notice of July 12, 2005, applicant hereby requests a pre-appeal brief review of this case for at least the following reasons. Claims 1-3 and 5-23 are pending.

Section 112 Rejection

Claim 1 stands rejected under Section 112, first paragraph. In particular, the Office Action contends that “connected directly in series” as recited in claim 1 is not supported by the specification as originally filed. This Section 112 rejection is respectfully traversed.

Claim 1 requires that (a) *the first and second PMOS transistors are connected directly in series*, and/or (b) *the first and second NMOS transistors are connected directly in series*. These recitations are supported by the instant specification as originally filed, at least via the figures thereof. For example and without limitation, figures of the instant application illustrate a cell

which includes PMOS section M05 comprising *PMOS transistors M05a and M05b connected directly in series*, and an NMOS section M06 including *NMOS transistors M06a and M06b connected directly in series* (e.g., see Figs. 2B, 5B, 10B, 13B-15B, etc.). The figures, which are part of the specification, clearly show and thus describe these features. There is no requirement that a feature shown in the drawings also be described in text – this would be virtually impossible in many instances. Thus, it is respectfully submitted that the instant specification supports the claim language which requires that (a) the first and second PMOS transistors are connected directly in series, and/or (2) the first and second NMOS transistors are connected directly in series.

The Section 112 rejection is improper and should be withdrawn.

Art Rejection

Claim 1 stands rejected under Section 102(e) as being allegedly anticipated by Yoon. This Section 102(e) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires that (a) *the first and second PMOS transistors are connected directly in series*, and/or (b) *the first and second NMOS transistors are connected directly in series*. This language in claim 1 prevents the Examiner from contending that in Fig. 6 of Yoon elements M16 and M19N are the claimed first and second NMOS transistors, and/or from contending that M15 and M19P are the claimed first and second PMOS transistors.

To summarize, Yoon fails to disclose or suggest that (1) *the first and second NMOS transistors are directly connected to each other in series* and/or (2) *the first and second PMOS transistors are directly connected to each other in series*, as required by claim 1. Instead, in Fig. 6 of Yoon, the PMOS transistor M15 of M16 and the PMOS transistor M19P are *not* connected directly in series; they are not connected directly in series because inverter devices M17, M18

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and driver-register circuit 618 are provided therebetween. Moreover, in Fig. 6 of Yoon, NMOS transistors M16 and M19N are not connected directly in series because driver-register circuit 618 is provided therebetween. Moreover, one of ordinary skill in the art would never have removed elements 618, M18 and M18 from Fig. 6 of Yoon.

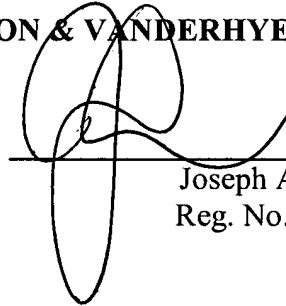
Conclusion

It is respectfully requested that all rejections be withdrawn. Claims 1, 6 and 8 are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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By:



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